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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,761	06/19/2001	Kazunobu Kuwazawa	15.44/5852	4015

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EXAMINER
ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/885,761	Applicant(s) KUWAZAWA, KAZUNOBU
	Examiner Stanetta D. Isaac	Art Unit 2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9 and 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al. US Patent 5,770,508.

3. Ma discloses the invention substantially as claimed. See Figs. **1a-3c** where Ma teaches a method for manufacturing a semiconductor device, the method comprising:

(a) forming a gate dielectric layer **12** over a semiconductor substrate;

(b) forming a gate electrode **14** over the gate dielectric layer;

(c) forming a dielectric layer **20** over the semiconductor substrate;

(d) forming a mask layer **23** over the dielectric layer;

(e) anisotropically etching the mask layer to form a sidewall mask layer **24** on sides of the gate electrode over the dielectric layer;

(f) isotropically etching the dielectric layer **22** using the sidewall mask layer as a mask to form an extension control layer and a sidewall protection layer on sides of the gate dielectric layer; and

(g) forming a first impurity layer **32** and a second impurity layer **34** by ion-implanting an impurity in the semiconductor substrate, wherein an extension region is formed in the

semiconductor substrate below the extension control layer during the ion-implanting used to form the first impurity layer and the second impurity layer.

4. Pertaining to claim 2, Ma teaches a method for manufacturing a semiconductor device according to claim 1, wherein the step (f) further includes the step of forming a sidewall protection layer on sidewalk of the gate electrode.

5. Pertaining to claim 3, Ma teaches a method for manufacturing a semiconductor device according to claim 2, further including removing the sidewall mask layer after the isotropically etching the dielectric layer and prior to the forming a first impurity layer and a second impurity layer.

6. Pertaining to claim 4, Ma teaches a method for manufacturing a semiconductor device according to claim 3, wherein the extension control layer is formed from a material comprising silicon nitride.

7. Pertaining to claim 5, Ma teaches a method for manufacturing a semiconductor device according to claim 4, wherein the sidewall mask layer is formed form a material comprising silicon oxide.

8. Pertaining to claim 6, Ma teaches a method for manufacturing a semiconductor device according to claim 3, wherein the extension control layer is formed from a material comprising silicon oxide.

9. Pertaining to claim 7, Ma teaches a method for manufacturing a semiconductor device according to claim 6, wherein the sidewall mask layer is formed from a sidewall.

10. Pertaining to claim 8, Ma teaches a method for manufacturing a semiconductor device according to claim 1, wherein the extension control layer has a thickness of 5-50 nm.

11. Pertaining to claim 9, Ma teaches a method for manufacturing a semiconductor device according to claim 3, wherein the sidewall mask layer is formed to a thickness of 30-200 nm.

12. Pertaining to claim 21, Ma teaches a method for manufacturing a semiconductor device including extension regions and source/drain regions formed using a single ion-implantation step, the method comprising:

forming a gate dielectric layer over a semiconductor substrate;

forming a gate electrode over the gate dielectric layer;

forming extension control structures over a portion of the semiconductor substrate next to the gate dielectric layer by forming a dielectric layer on the semiconductor substrate,

forming a mask layer on the dielectric layer, anisotropically etching the mask layer to form a sidewall mask layer, and isotropically etching the dielectric layer after forming the sidewall mask layer; and

an ion-implanting step that forms extension regions in the semiconductor substrate under the extension control structures and source/drain regions in the semiconductor substrate adjacent to the extension layer, wherein the extension regions have a depth that is less than that of the source/drain regions.

13. Pertaining to claim 22, Ma teaches a method according to claim 21, further comprising forming sidewall protection structures on sidewalk of the gate electrode during the isotropically etching the dielectric layer.

14. Pertaining to claim 22, Ma teaches a method according to claim 22, further comprising removing the sidewall mask layer prior to the ion-implanting.

15. Pertaining to claim 24, Ma teaches a method of manufacturing a semiconductor device according to claim 1, wherein the extension control layer is formed from silicon nitride and the sidewall mask is formed from silicon oxide.

16. Pertaining to claim 25, Ma teaches a method according to claim 21, wherein the ion-implanting step is carried out as a single ion-implantation operation.

17. Pertaining to claim 26, Ma teaches a method according to claim 22, wherein the extension control layer and the sidewall protection layer are formed from silicon nitride and the sidewall mask layer is formed from silicon oxide.

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

19. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 703-308-5871. The examiner can normally be reached on Monday-Friday 7:30am -5:30pm.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Nebling can be reached on 703-308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-3432 for After Final communications.

22. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Stanetta Isaac
Patent Examiner
May 14, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800